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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,795	12/29/2000	Robert D. Wachel	2207/9069	5317

25693 7590 11/07/2002

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EXAMINER

VIGUSHIN, JOHN B

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 11/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/751,795

Applicant(s)

WACHEL, ROBERT D.

Examiner

John B. Vigushin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 29 December 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-13, 19 and 20 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4-9 and 14 is/are rejected.
- 7) ☒ Claim(s) 3 and 15-18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

**Rejections Based On Prior Art**

1. The following reference was relied upon for the rejections hereinbelow:

Granau et al. (US 5,848,252)

***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 6-9 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Granau et al.

As to Claim 1, Granau et al. discloses plural PCI segments (one segment being the row array of slot connectors 303 and the other segment being the row array of slot connectors 305; col.2: 6-13; col.3: 25-28), and PCI cards mounted in slots 303 and 305 on a PCI chassis comprising backplane circuit panels 101 and 103 (Figs. 2 and 3); a bridge for coupling the PCI segments, the bridge comprising: a board 301; connectors 307 and 309 mounted on board 301 for electrically connecting board 301 to a first PCI segment (the row array of connectors 303) and a second PCI segment (the row array of connectors 305) on a backplane (defined by circuit panels 101 and 103) of the PCI chassis (Fig. 3; col.3: 15-33).

As to Claim 2, Granau et al. further discloses that the plurality of connectors 307 and 309 are J1 and J2 (female) connectors (Fig. 3).

As to Claim 6, Granau et al. further discloses that board 301 electrically connects to the first and second PCI segments in adjacent slots 303 and 305 on the PCI chassis (Fig. 3; "adjacent" in that slots 303 and 305 are next to each other in a collinear configuration).

As to Claim 7, Granau et al. further discloses that board 301 electrically connects to the first and second PCI segments in non-adjacent slots 303 and 305 on the PCI chassis (Fig. 3; "non-adjacent" in that slots 303 and 305 are not parallel, i.e., adjacent, to each other).

As to Claim 8, Granau et al. further discloses that board 301 is configured to mount on the backplane (defined by circuit panels 101 and 103) of the PCI chassis in the slot occupied by a transition card, as evidenced by connector 311 which allows programming the system processor on the board 301 from an external programming source (see col.3: 11-13 which describes connector 213, which is the same type of connector in the embodiment of Fig. 2 as connector 311 in the Fig. 3 embodiment; also see Applicant's description of a "transition card" on p.7, line 17-p.8, line 1).

As to Claim 9, Granau et al. further discloses, in Fig. 3, that connectors 307 and 309 connect only to groups of P1 pins (connector 303) and P2 pins (connector 305).

As to Claim 14, Granau et al. discloses, in Fig. 3, connecting a first PCI segment slot 303 and a second PCI segment slot 305 with a first bridge card 301 (col.3: 25-28); locating the bridge card 301 along a backplane (defined by circuit panels 101 and 103).

***Claim Rejections - 35 USC § 102(b)/103(a)***

4. Claims 4 and 5 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Granau et al. in view of Applicant's admitted prior art.

A) 35 USC § 102(b) rejection:

As to Claims 4 and 5, Granau et al. further discloses a processor 109 mounted on board 301 (board 301 being the single board version of the cable-connected boards 201 and 203 from the embodiment of Fig. 2, wherein the system processor 109 is located on one or both bridge boards 201 and 203; inherently processor 109 is incorporated into the single bridge board 301 for the Fig. 3 embodiment; col.2: 65-col.3: 3; col.3: 15-33) and electrically connected to the plurality of connectors 307 and 309, wherein the processor 109 logically connects the first and second PCI segments with a transparent bridge or, alternatively, a non-transparent bridge; i.e., the processor 109 on bridge board 301, as used in conjunction with the bus host, enables the PCI Buffered Interfaces 105 and 107 to provide "a communication means and communication isolation between the two connected PCI Buses 101 and 103 (col.2: 26-31 and 48-55)." When a "communication means" on bridge board 301 is provided between the PCI bus segments on circuit panels 101 and 103--i.e., in an application wherein "two-way transfer/conversion of data between two independent buses is required [col.2: 49-50]," the bridge protocol on bridge board 301 with which the processor 109 logically connects the first and second PCI bus segments must inherently be *transparent*. When "communication isolation" between the PCI segments is provided--i.e., in an application

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wherein one PCI segment is a "secure" bus segment while the other is an "open" bus segment (col.2: 50-53)--then the bridge protocol on bridge board 301 with which the processor 109 logically connects the first and second PCI bus segments must inherently be *non-transparent* (see col.2: 6-55 for a more complete description of the bridge functions on bridge board 301 and the role played by processor 109).

B) 35 USC § 103(a) rejection:

As to Claims 4 and 5:

la. Granau et al. discloses a processor 109 mounted on board 301 (board 301 being the single board version of the cable-connected boards 201 and 203 from the embodiment of Fig. 2, wherein the system processor 109 is located on one or both bridge boards 201 and 203; inherently processor 109 is incorporated into the single bridge board 301 for the Fig. 3 embodiment; col.2: 65-col.3: 3; col.3: 15-33) and electrically connected to the plurality of connectors 307 and 309, wherein the processor 109 logically connects the first and second PCI bus segments of circuit panels 101 and 103 with a bridge circuit on bridge card 301 (col.2: 26-31 and 48-55).

lb. Moreover, Granau et al. further teaches that the processor 109 on bridge board 301, as used in conjunction with the bus host, enables the PCI Buffered Interfaces 105 and 107 to provide both "a communication means and communication isolation between the two connected PCI Buses 101 and 103 (col.2: 26-31 and 48-55)." Specifically, Granau et al. teaches that: **(1)** a "communication means" is provided between the PCI bus segments on circuit panels 101 and 103 in an application wherein "two-way transfer/conversion of data between two independent buses is required [col.2:

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49-50];” and that **(2)** “communication isolation” is provided between the PCI segments in an application requiring one-way transfer and encryption of data from one “secure” PCI bus segment to the other “open” PCI bus segment (col.2: 50-53).

II. Granau et al. does not specify the bridge protocol used; i.e., transparent or non-transparent with which the processor 109 logically connects the first and second PCI bus segments.

III. Applicant’s admitted prior art discloses that *transparent* and *non-transparent* busses are old and well-known bus protocols in the art that are used to connect first and second PCI bus segments (see the *Specification: p.9, lines 12-18* of the instant Application).

IV. Since Granau et al. discloses applications wherein a bridge board 301 with processor 109 serves to bridge busses that freely interchange data between devices on both busses (e.g., application **(1)**), and applications wherein a bridge board 301 with processor 109 serves to bridge busses that exhibit only one-way transfer of data (e.g., application **(2)**), then it would have been obvious to one of ordinary skill in the art at the time the invention was made: **(i)** for the processor 109 on bridge board 301 to logically connect the first and second PCI bus segments with a *transparent* bridge (e.g., in application **(1)**), as is well-known in the art, so that all peripheral devices on both busses are addressable as on a single logical bus, thus reducing the amount of bus cycles needed to complete a transaction and thereby simplifying and speeding-up data transfer between the system’s peripheral devices; and **(ii)** for the processor 109 on bridge board 301 to logically connect the first and second PCI bus segments with a *non-transparent*

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bridge (e.g., in application (2)), as is well-known in the art, so that peripheral components and other devices on the secure bus are not discovered by the peripherals and other devices on the open bus.

***Allowable Subject Matter***

5. Claims 10-13 and 19-20 have been allowed.
6. Claims 3 and 15-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
7. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 3, patentability resides in *the bridge board having four connectors for connection to the P1 and P2 groups of pins of the first and second PCI segments*, in combination with the other limitations of the claim.

As to Claims 10-13, patentability resides in *a system including at least three PCI segments wherein the bridge comprises a second board with connectors for electrically connecting the second board to a second and third PCI segment on the PCI chassis backplane*, in combination with the other limitations of base Claim 10.

As to Claim 15, patentability resides in *mounting the PCI bridge card in a notch between the PCI chassis and a transition card*, in combination with the other limitations of the claim.

As to Claims 16-18, patentability resides in *connecting a second PCI segment slot and a third PCI segment slot with a second PCI bridge card*, in combination with the other limitations of the broadest claim, Claim 16.

As to Claims 19-20, patentability resides in *orienting the PCI bridge card substantially parallel to the PCI chassis*, in combination with the other limitations of base Claim 19.

8. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

### **Conclusion**

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Draughn et al. (US 6,349,037 B1) discloses adapter cards F and G with primary bus connectors a'7, 'a'8, respectively, and secondary bus connectors b'7, b'8, respectively, connected to connectors a7, a8 and b7, b8 on the primary backplane A (Fig. 1; col.3: 58-64) for use in a device including a bridge (col.4: 2-10) and having PCI bus structure (col.2: 48-54 and 60-61).

b) Gallick et al. (US 6,282,599 B1) discloses a cabinet chassis having a PCI bridge card used in a compact PCI (cPCI) backplane (Figs. 2 and 3; col.3: 15-57).

c) Lanus et al. (US 6,112,271) discloses bridge boards (1) and (2) used in a multiconfiguration backplane including a compact PCI bus (Figs. 1-5; col.2: 8-22).

d) Crane, Jr. et al. (US 6,092,139) discloses a bridge card 530 attached to a backplane and receiving signals from various devices through PCI and ISA busses (Fig. 10; col.15: 44-64).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



John B. Vigushin  
Examiner  
Art Unit 2827

jbv  
November 5, 2002